What is claimed is:

1. A method for driving a plasma display panel method in which successive field periods, each including a reset period for initializing the state of respective cells, an address period for selectively discriminating cells to be turned on from cells not to be turned on and for performing an addressing operation, and a sustain period for discharging the addressed cells, are performed, and a reset stabilization period for inducing discharging in a discharge space between cells is additionally performed before the reset period if a rest period having a predetermined time duration is present between the sustain period of a preceding field and the reset period of the field.

2. The method of claim 1, wherein, in the reset stabilization period, discharging is induced in the cells discharged in the sustain period of the preceding field.

3. The method of claim 1, wherein, in the reset stabilization period, at least one of the number of discharging occurrences, the width of discharge pulses, or the level of a discharge pulse voltage is varied depending on the duration of the rest period.

4. A method of driving a plasma display panel for displaying a picture by causing discharging in a discharge space between electrodes, in which if there is a time interval during which no discharging occurs in the discharge space before a reset period, a reset stabilization period is additionally performed before the reset period by applying a predetermined voltage to the electrodes to cause discharging between the electrodes.

5. The method of claim 4, wherein, in the reset stabilization period, discharging is induced in the cells discharged in a sustain period.

6. The method of claim 4, wherein, in the reset stabilization period, at least one of the number of discharging occurrences, the width of discharge pulses, or the level of a discharge

pulse voltage is varied depending on the duration of the time interval during which no discharging occurs before the reset period.

7. A method of driving a plasma display panel driving in which successive field periods, each including a reset period for initializing the state of respective cells, an address period for selectively discriminating cells to be turned on from cells not to be turned on and for performing an addressing operation, and a sustain period for discharging the addressed cells, are performed, and a rest period in which no discharge in the cells occurs for a predetermined time is positioned between the reset period and the address period, between the address period and the sustain period, or in the middle of the sustain period or the address period.

8. The method of claim 7, wherein the rest period is temporally divided and then distributed in the address period or the sustain period.

9. A plasma display panel driving apparatus, comprising:

a reset signal generator for generating a reset signal initializing the state of respective cells;

an address signal generator for generating an address signal selectively discriminating cells to be turned on from cells to be turned off and for performing an addressing operation; and

a sustain signal generator for generating a sustain signal discharging the cells addressed by the address signal generator,

wherein if cell discharging does not occur for a predetermined time interval before application of the reset signal, the reset signal generator generates a reset stabilization signal to cause discharging to occur in the cells prior to the generation of the reset signal.

10. A plasma display panel driving apparatus comprising:

a reset signal generator for generating a reset signal initializing the state of respective cells in a reset period;

an address signal generator for generating an address signal selectively discriminating cells to be turned on from cells not to be turned on and for performing an addressing operation in an address period;

a sustain signal generator for generating a sustain signal discharging the cells addressed by the address signal generator in the sustain period; and

a signal synthesizer for applying the reset signal, the address signal, and the sustain signal to electrodes,

wherein if a rest period lasting for a predetermined length of time during which no cell discharging occurs is present in a field consisting of the reset period, the address period, and the sustain period, the signal synthesizer synthesizes the reset signal, the address signal, and the sustain signal such that the rest period is positioned between the reset period and the address period, between the address period and the sustain period, or in the middle of the sustain period or the address period.

11. A method of driving a plasma display panel in which a reset period for initializing the state of respective cells, an address period for selectively discriminating cells to be turned on from cells not to be turned on and for performing an addressing operation, a sustain period for discharging the addressed cells in the address period, and a reset stabilization period, if a rest period having a predetermined time duration follows the sustain period, for causing discharging in a discharge space between cells before a next reset period, are performed.

12. The method of claim 11, wherein, in the reset stabilization period, a predetermined number of reset pulses that are substantially the same as pulses applied to electrodes in the sustain period are applied.

13. The method of claim 11, wherein reset pulses applied in the reset period comprise a square pulse applied in an early stage of the reset period and a ramp pulse applied in a latter stage of the reset period with a gradually decreasing voltage level.

14. The method of claim 13, wherein, in the reset period, the reset pulses are applied to scan electrodes and a constant voltage is applied to sustain electrodes.

15. The method of claim 11, wherein reset pluses applied in the reset period comprise a first ramp pulse applied in an early stage of the reset period with a gradually increasing voltage level and a second ramp pulse applied in a latter stage of the reset period with a gradually decreasing voltage level.